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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Christopher J. Diorio et al.

Title: MULTI-OSCILLATOR CLOCK SIGNALS

Docket No.: 2051.007US1

Filed: April 13, 2004

Examiner: Vernal Brown

Serial No.: 10/824,048

Due Date: N/A

Group Art Unit: 2612


Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the attached:

- ☒ Communication Re: Incorrect Filing Receipt (1 pg.)
- ☒ Copy of Filing Receipt (2 pgs.)
- ☒ Copy of the Office Action Amendment and Response filed March 13, 2006 (10 pgs.)
- ☒ A return postcard.

No Additional fee is required.

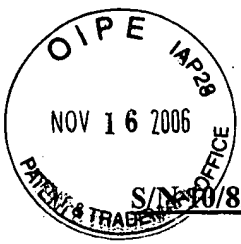
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Customer No: 21186

By: 
Name: Andre L. Marais
Reg. No. 48,095
ALM:CMG:njc

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Nancy Cournoyer
Name

Nancy Cournoyer
Signature



S/N 10/824,048

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Christopher J. Diorio et al.	Examiner:	Vernal Brown
Serial No.:	10/824,048	Group Art Unit:	2612
Filed:	April 13, 2004	Docket:	2051.007US1
Customer No.	21186	Confirmation No.	6115
Title:	MULTI-OSCILLATOR CLOCK SIGNALS		

COMMUNICATION RE: REQUEST FOR UPDATE FILING RECEIPT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants hereby request an updated Filing Receipt with respect to the above-identified patent application. In the Filing Receipt received September 10, 2004, (copy enclosed), shows the title **"METHOD AND SYTEM TO GENERATE MODULATOR AND DEMODULATOR CLOCK SIGNALS WITHIN AN RFID CIRCUIT UTLIZING A MULTI-OCCILLATOR ARCHITECTURE"**

The title has been amended to: **"MULTI-OSCILLATOR CLOCK SIGNALS"** as of the Office Action Amendment and Response filed March 13, 2006, (copy enclosed).

Applicants would appreciate the above-identified printing error be corrected and that a new "corrected" filing receipt be sent to Applicants' representatives at the address given below.

Respectfully submitted,


CHRISTOPHER J. DIORIO ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
408-278-4042

Date November 13, 2006

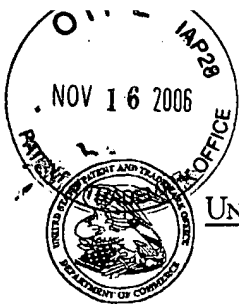
By /


Andre L. Marais
Reg. No. 48,095
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NANCY Cournoyer
Name

Nancy Cournoyer
Signature



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/824,048	04/13/2004	2635	986	6928P010	17	19	4

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SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

PROCESSED BY
DOMESTIC
ADMINISTRATOR

CONFIRMATION NO. 6115

UPDATED FILING RECEIPT



OC000000013778470

Date Mailed: 09/10/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Christopher J. Diorio, Shoreline, WA;
Vadim Gutnik, Irvine, CA;
Todd E. Humes, Shoreline, WA;

RECEIVED

SEP 13 2004

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
LOS ANGELES

Power of Attorney: The patent practitioners associated with Customer Number **45064**.

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 06/24/2004

The number of your priority application, to be used for filing abroad under the Paris Convention is,
US10/824,048

Projected Publication Date: 10/13/2005

Non-Publication Request: No

Early Publication Request: No

ENTERED

SEP 17 2004

STATUS

Title

Method and system to generate modulator and demodulator clock signals within an RFID circuit utilizing a multi-oscillator architecture

Preliminary Class

340

**LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

GRANTED

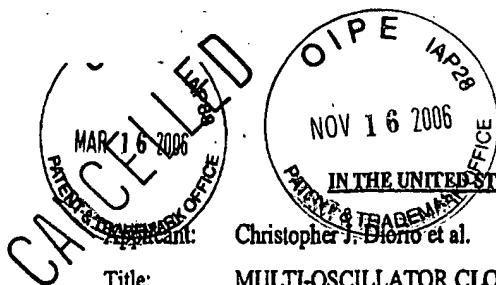
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X vv

Applicant: Christopher J. Diono et al.

Title: MULTI-OSCILLATOR CLOCK SIGNALS (As Amended)

Docket No.: 2051.007US1

Serial No.: 10/824,048

Filed: April 13, 2004

Due Date: March 14, 2006

Examiner: Vernal Brown

Group Art Unit: 2635

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ Return postcard.
- ☒ Amendment and Response (13 pgs.).
- ☒ Authorization to charge the Deposit Account No. 19-0743 in the amount of \$250.00 to cover the fee for additional claims as calculated below.

If not provided for in a separate paper filed herewith, if an additional fee is required due to changes to the claims, the fee has been calculated as follows:

CLAIMS AS AMENDED					
	(1) Claims Remaining After Amendment	(2) Highest Number Previously Paid For	(3) Present Extra	Rate	Fee
TOTAL CLAIMS	20	19	1	x 50 =	\$50.00
INDEPENDENT CLAIMS	5	4	1	x 200 =	\$200.00
[] MULTIPLE DEPENDENT CLAIMS PRESENTED					\$0.00
TOTAL					\$250.00

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Customer Number 21186

By: Mark V. Muller
Atty: Mark V. Muller
Reg. No. 37,509

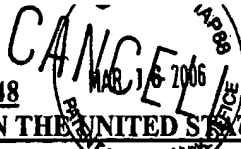
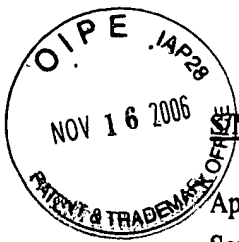
CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this day of March, 2006. 13

Name: Dawn R. Shaw

Signature: Dawn R. Shaw

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)

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SN 10/824,048

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Christopher D. D'Orio et al.

Examiner: Vernal Brown

Serial No.: 10/824,048

Group Art Unit: 2635

Filed: April 13, 2004

Docket No.: 2051.007US1

Title: MULTI-OSCILLATOR CLOCK SIGNALS (As Amended)

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This communication responds to the Office Action mailed on December 14, 2005. Please amend the above-identified patent Application as follows, and consider the appended remarks.

03/20/2006 NHUYEN1 00000003 190743 10824048

01 FC:1201 200.00 DA
02 FC:1202 50.00 DA

IN THE TITLE

Please delete the current Title in its entirety and substitute the following in its place:

MULTI-OSCILLATOR CLOCK SIGNALS

IN THE SPECIFICATION

Please delete the current Abstract of the Disclosure in its entirety and substitute the following in its place:

ABSTRACT OF THE DISCLOSURE

Methods and apparatus may operate to use multiple oscillators to generate a demodulator clock signal and a modulator clock signal within a radio-frequency identification (RFID) circuit. The demodulator clock signal may be generated from a radio-frequency signal received at the RFID circuit. A modulator clock signal may be generated using a calibration value stored in a non-volatile memory.

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) ~~An~~ A radio-frequency identification (RFID) circuit for use within an RFID tag, the circuit including:

first clock generation circuitry to generate a modulator clock signal using a first oscillator within the RFID circuit, the modulator clock signal being generated utilizing a first calibration value stored within a non-volatile memory associated with the ~~RFID tag~~ RFID tag; and

second clock generation circuitry to generate a demodulator clock signal using a second oscillator within the RFID circuit, the demodulator clock signal being recovered from a ~~radiofrequency~~ radio-frequency signal received at the RFID tag.

2. (Currently Amended) The circuit of claim 1, ~~wherein the second clock generation circuitry includes a second oscillator, and~~ wherein the second clock generation circuitry is to recover a clock signal from the radio-frequency signal received at the RFID tag, to compare the recovered clock signal to an oscillator clock signal generated by the second oscillator ~~of the RFID circuit~~, and to store a second calibration value, based on the difference between the recovered clock signal and the oscillator clock signal, within a memory device associated with the RFID circuit.

3. (Currently Amended) The circuit of claim 2, wherein the second clock generation circuitry includes calibration circuitry to calibrate the second oscillator ~~of the RFID circuit~~ utilizing the second calibration value.

4. (Original) The circuit of claim 2, wherein the second calibration value is stored within a volatile memory associated with the RFID tag.

5. (Currently Amended) The circuit of claim 1, wherein the first clock generation circuitry ~~includes a first oscillator, and~~ is to retrieve the first calibration value from the non-volatile

memory associated with the RFID tag, and to generate the modulator clock signal by calibrating in the first oscillator utilizing the first calibration value.

6. (Original) The circuit of claim 1, wherein the first clock generation circuitry is to generate a system clock signal based on the first calibration value stored within the non-volatile memory associated with the RFID tag.

7. (Currently Amended) A method of generating a demodulator clock signal and a modulator clock signal within ~~an~~ a radio-frequency identification (RFID) circuit for use within an RFID tag, the method including:

generating a modulator clock signal utilizing a first oscillator included in the RFID circuit and a first calibration value stored within a non-volatile memory associated with the RFID tag;
and

generating the demodulator clock signal from a radio-frequency signal received at the RFID tag using a second oscillator included in the RFID circuit.

8. (Currently Amended) The method of claim 7, wherein the generating of the demodulator clock signal includes recovering a clock signal from the radio-frequency signal received at the RFID tag, comparing the recovered clock signal to an oscillator clock signal generated by the a ~~second oscillator of the RFID circuit~~, and storing a second calibration value, based on the difference between the recovered clock signal and the oscillator clock signal, within a memory device associated with the RFID tag.

9. (Currently Amended) The method of claim 8, wherein the generating of the demodulator clock signal includes calibrating the second oscillator ~~of the RFID circuit~~ utilizing the second calibration value.

10. (Original) The method of claim 8, wherein the second calibration value is stored within a volatile memory associated with the RFID tag.

11. (Currently Amended) The method of claim 7, including retrieving the first calibration value from the non-volatile memory associated with the RFID tag, wherein the generating of the modulator clock signal includes calibrating the a first oscillator of the RFID circuit utilizing the first calibration value.

12. (Original) The method of claim 7, including generating a system clock signal based on the first calibration value stored within the non-volatile memory associated with the RFID tag.

13. (Currently Amended) ~~An~~ A radio-frequency identification (RFID) circuit for use within an RFID tag, the circuit including:

first means for generating a modulator clock signal using a first oscillator within the RFID circuit, the modulator clock signal being generated utilizing a first calibration value stored within a non-volatile memory associated with the RFID tag; and

second means for generating a demodulator clock signal within the RFID circuit, the demodulator clock signal being recovered from a radio-frequency ~~signal received~~ signal received at the RFID tag using a second oscillator included in the RFID circuit.

14. (Currently Amended) A machine-readable medium storing a description of ~~an~~ a radio-frequency identification (RFID) circuit for use in an RFID tag, said RFID circuit comprising:

first clock generation circuitry to generate a modulator clock signal using a first oscillator within the RFID circuit, the modulator clock signal being generated utilizing a first calibration value stored within a non-volatile memory associated with the RFID tag; and

second clock generation circuitry to generate a demodulator clock signal within the RFID circuit, the demodulator clock signal being recovered from a radio-frequency signal received at the RFID tag using a second oscillator included in the RFID circuit.

15. (Original) The machine-readable medium of claim 14, wherein the description comprises a behavioral level description of the circuit.

16. (Currently Amended) The machine-readable medium of claim 15, wherein the behavioral level description is compatible with a very high speed integrated circuit (VHSIC) hardware description language (VHDL) format.
17. (Currently Amended) The machine-readable medium of claim 15, wherein the behavioral level description is compatible with a Verilog hardware description language format.
18. (Original) The machine-readable medium of claim 14, wherein the description comprises a register transfer level netlist.
19. (Original) The machine-readable medium of claim 14, wherein the description comprises a transistor level netlist.
20. (New) An apparatus, including:
 - a radio-frequency identification (RFID) tag; and
 - a circuit included in the RFID tag, the circuit including a first oscillator and first clock generation circuitry to generate a modulator clock signal within the circuit, the modulator clock signal being generated utilizing a first calibration value stored within a non-volatile memory included in the RFID tag, and second clock generation circuitry to generate a demodulator clock signal within the circuit, the demodulator clock signal being recovered from a radio-frequency signal received at the RFID tag using a second oscillator included in the circuit.

In summary, none of the references disclose an apparatus having "a first oscillator" and "a second oscillator" in the RFID circuit, as claimed by the Applicant. There is no motivation to combine the references (in fact, the AAPA and Roesner both teach away from the suggested modification), and no reasonable expectation of success results from their combination. The requirements of *M.P.E.P.* § 2142 have not been satisfied, and a *prima facie* case of obviousness has not been established. It is therefore respectfully requested that the rejections to claims 1-13 under 35 U.S.C. § 103 be reconsidered and withdrawn.

CONCLUSION

The Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicant's attorney, Mark V. Muller at 210-308-5677 to facilitate prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

CHRISTOPHER J. DIORIO ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
210 308-5677

Date March 13, 2006

By Mark V. Muller
Mark V. Muller
Reg. No. 37,509

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Dawn R. Shaw

Name

Dawn R. Shaw
Signature